REMARKS

Claims 8, 9, 12-15, 17, 19-21 and 30-32 are pending in the present application, were examined, and stand rejected. In response, Claims 8, 15, 19 and 30 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 8, 9, 12-15, 17, 19-21 and 30-32 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §101

The Examiner has rejected Claims 8-9, 12-13 and 30-32 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. In response, Applicants have amended Claim 8 to recite the following claim feature to provide a tangible result:

> populating entries within a conversion table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses. (Emphasis added.)

Applicants respectfully submit that the population of entries within the conversion table provides a tangible result, which is useful for address translation from virtual addresses of an allocated memory range to physical addresses for access to main memory; specifically, providing physical addresses have a greater number of bits than the virtual addresses of an allocated memory range enables access to memory above a register/bus width limit, such as, for example, a 4 gigabit (Gb) limit imposed by 32-bit register/bus width.

Accordingly, in view of Applicants' amendments to Claim 8, Applicants respectfully submit that the population of entries within the conversion table provides a practical application that produces a useful concrete and tangible result of accessing memory above, for example, the four Gb limited imposed by 32-bit register/bus width, in accordance with State Street and Trust Co. v. Signature Financial Groups, Incorporated, 149 F.3d 1368. Therefore, Applicants respectfully submit that Claim 8, as amended, is directed to statutory subject matter in compliance with 35 U.S.C. §101.

Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §101 rejection to Claim 8, as well as Claims 9 and 12-13, based on their dependency from Claim 8.

Regarding Claim 30, Claim 30 recites an apparatus comprising a translation control circuit, which programs entries of the translation lookaside buffer to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses. Applicants respectfully submit that the rejection of Claim 30 is wrong as a matter of law without amendment. These are apparatus claims and are structured. The 35 U.S.C. §101 rejection is proper regarding method claims and not apparatus claims, such as Claim 30. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §101 rejection of Claims 30 and dependent Claims 31 and 32.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 8-9, 12-14 and 30-32 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,477,623 ("Jeddeloh") in view of U.S. Patent No. 6,526,459 issued to Campbell ("Campbell").

Regarding Claim 8, Claim 8 is amended to recite the claim feature, which is neither taught nor suggested by the combination of Jeddeloh in view of Campbell:

> populating entries within a conversion table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses. (Emphasis added.)

As correctly noted by the Examiner, Jeddeloh does not disclose the second address having a greater number of bits than the first address and the fourth address having a greater number of bits than the third address, as recited by amended Claim 8. As a result, the Examiner cites Campbell. As indicated by the Examiner:

> Campbell teaches a conversion table (TLB; C 3, L 32-34) to translate a first address to a second address, wherein the second address has a greater number of bits than the first address (C 3, L 37-42). This feature taught by Campbell provides flexible address space allocation. Hence, it would have been obvious to one of ordinary skill in the art to incorporate Campbell's teachings with the system taught by Jeddeloh for the desirable purpose of efficiency and flexibility. (pg. 3, ¶2 – pg. 4, ¶1 of the Office Action mailed March 13, 2006.)

Regarding Campbell, Campbell teaches a translation lookaside buffer that remaps access to internal I/O devices from a virtual address space, for I/O bus-based I/O devices, to a physical address space for internal I/O devices. (*See*, Abstract.) As taught by Campbell:

> An embodiment of the present invention allows the limitations of the PCI bus to be overcome while still providing compatibility with software intended for use with PCI-bus-based I/O devices. This embodiment preserves the software image of the I/O devices as PCI-bus-based I/O devices, but allows communication with the I/O devices to bypass the PCI bus. This embodiment also allows circuitry for interfacing with the I/O devices separately from the PCI bus to be fabricated as a single integrated circuit device along with the other system components, such as central processing unit (CPU). (col. 2, lines 29-39.) (Emphasis added.)

To provide such functionality, Campbell teaches, with reference to FIG. 5, the allocation of different address spaces to different types of addressing usage including DRAM 501, PCI memory 502, PCI I/O 503 and internal devices 504. Applicants respectfully submit that the additional bits of the physical address shown in FIG. 3, which are used to identify different address spaces allocated to different types of addressing usage, do not enable access above the memory limit imposed by the prior art I/O address mapping, as shown in FIG. 4.

As shown in FIG. 5, the various address spaces are provided to enable access to the respective device and not to main memory. As known to those skilled in the art, the I/O address spaces referred to by Campbell map a portion of the system address space for access to one or more I/O devices. As a result, a portion of the system address space is interpreted as access to a device rather than access to main memory. (*See*, for example, process block 608 and 609 of FIG. 6 and process blocks 804 and 805 of FIG. 8 of Campbell.)

As taught by Campbell:

> The invention uses the TLB to remap virtual addresses usually associated with external I/O devices to internal device address space 504. This allows internal I/O devices to emulate external I/O devices, thereby providing compatibility of internal I/O devices with software programmed to interact with external I/O devices. (col. 4, lines 60-65.) (Emphasis added.)

Providing this capability enables Campbell to support I/O devices that do not closely conform to the PCI standard. (col. 1, lines 51-52.) As further taught by Campbell:

> DMA engine 206 allows DMA operations to be performed with respect to DRAM memory device 214 without the need for intervention by the CPU 203. (col. 3, lines 7-19.) (Emphasis added.)

Applicants respectfully submit that Campbell is devoid of any disclosure, teaching or suggestion of the DMA engine 206 using TLB 204 to perform translations between virtual addresses and physical addresses for access to DRAM memory device 214 since the DMA engine 206 allows DMA operations to be performed with respect to the memory device 214 without the need for intervention by CPU 203; CPU 200 utilizes virtual addresses in a virtual memory space in spite of the fact that the memory device is organized according to physical addresses in physical memory space. (*See*, col. 3, lines 15-19.)

Conversely, Claim 8 as amended, populates entries within a conversion table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses. As mandated by case law, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Here, Jeddeloh is completely devoid of, and fails to teach or suggest, expansion of a physical address range for access to main memory. Instead of modification to a translator physical address range for access to main memory, the teachings of Jeddeloh are specifically limited to avoiding bandwidth constraints imposed on data transfers between the processor and graphics controller due to busses and/or data channels that couple these components together. (*See*, col. 1, lines 57-61.)

Furthermore, the only mention of address translation within Jeddeloh occurs at col. 6, wherein it is indicated that GART table 202 performs address translation on the fly, as data transfers traverse switch 124, such that addresses that fall within a reserve range are delayed so that address translation can take place. (*See*, col. 6, lines 51-67.) In fact, Jeddeloh fails to teach or suggest how this address translation is performed and simply refers to the address translation without providing any details as to how such translation is performed.

Conversely, Campbell is directed to rectifying a number of disadvantages, which arise from I/O address space allocation according to the PCI memory address space 402, as shown in FIG. 4, to enable support for I/O devices that do not closely conform to the PCI standard. As a result, rather than limiting I/O address space mapping, for example as shown in FIG. 4, Campbell discloses the use of several different addresses spaces allocated to the different types

of addressing usage by providing additional bits as part of a physical address. (col. 3, lines 28-42.)

However, the providing of the additional address spaces is not performed to provide or expand the physical address range beyond, for example, the 4 Gb limit imposed by 32-bit I/O devices. Campbell teaches the remapping of virtual addresses associated with external devices to an internal device address space to allow internal I/O devices to emulate external I/O devices. Remapping, as taught by Campbell, provides compatibility of internal I/O devices with software program to interact with external I/O devices, such as PCI devices. (col. 4, lines 60-65.)

Consequently, Applicants respectfully submit that the combination of Jeddeloh in view of Campbell fails to teach or suggest at least the population of a conversion table to map virtual addresses of a virtual address range allocated to a graphics controller to physical addresses of main memory, wherein the physical addresses have a greater number of bits than the virtual addresses, as recited by amended Claim 8 and required to establish *prima facie* obviousness. Id.

Moreover, the teachings of Jeddeloh in view of Campbell would not have suggested modification of the address translation using the GART table of Jeddeloh to extend the physical address space for access to main memory, as recited by amended Claim 8, since the teachings of Jeddeloh are specifically limited to addressing the following problems described in the Background of Jeddeloh:

> Data transfers between processor and graphics controller, and between graphics controller and system memory are presently constrained by the bandwidth of the busses and their data channels that couple these components together. (col. 1, lines 56-60.) (Emphasis added.)

As specifically indicated in the Background of Jeddeloh, what is needed is a computer system that facilitates high bandwidth data transfers between a graphics controller and other system components. (*See*, col. 2, lines 11-13.) To achieve this goal, Jeddeloh teaches data paths, which connect the graphics controller and other devices to switch 124 (FIG. 2) to have a greater width than busses that typically couple computer system components together.

In other words, the teachings of Jeddeloh are directed to provided high bandwidth communications and are not directed to physical address range limitations caused by bus and register widths for accessing memory above the four gigabit limit imposed by a 32-bit bus and register widths. Furthermore, the teachings of Campbell are limited to disadvantages, which arise from allocating an address space as dictated by the PCI standard, which is heavily

constrained, and therefore makes it difficult to support I/O devices that do not closely conform to the PCI standard. (Col. 1 lines 41-52.) Therefore, Campbell is also not directed to providing I/O devices with access to main memory above, for example, the 4 Gb limit imposed by 32-bit register/bus widths.

Consequently Applicants respectfully submit that the Examiner has established obviousness by combining the teachings of prior art to produce the features recited by amended Claim 8 in spite the absence of a teaching or suggestion supporting such combination. ACS Hospice, Inc. v. Montefiore Hosp, 732 F.2d 1572, 1577, 221 USPQ 929, 939 (Fed. Cir. 1984) Hence, Applicants respectfully submit that the Examiner has found obviousness through hindsight to construct the features of amended Claim 8 from the elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (C.C.P.A. 1967.)

Therefore, for these reasons provided above Applicants respectfully submit that the combined teachings of Jeddeloh in view of Campbell fail to teach or suggest each of the above-recited features of amended Claim 8 as required to establish a *prime facie* case of obviousness. In re Royka, supra. Furthermore, applicants respectfully submit that the Examiner has engaged a prohibited hindsight-based analysis to find obviousness of amended Claim 8 from elements of the prior art in spite of the absence of a teaching or suggestion supporting such combination. In re Warner, supra.

Therefore, for these reasons provided above amended Claim 8 is patentable over the combination of Jeddeloh in view of Campbell. Consequently, Applicants respectfully request the Examiner reconsider and withdraw the §103 rejection of amended Claim 8.

Regarding Claim 9 and 12-14, Claim 9 and 12-14 based on their dependency from Claim 8 are also patentable over the combination of Jeddeloh in view of Campbell. Therefore, Applicants respectfully request the Examiner reconsider and withdraw the §103 rejection of Claim 9 and 12-14.

Regarding Claim 30, Claim 30 is amended to recite the following claim features which are neither disclosed, taught nor suggested by the combination of Jeddeloh in view of Campbell:

> a translation control circuit coupled to the address translator to program entries in the translation lookaside buffer entries to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses. (Emphasis added.)

For at least the reasons indicated above, Applicants respectfully submit that the combination of Jeddeloh in view of Campbell fails to teach or suggest the programming of entries in a translation lookaside buffer to map virtual address of a virtual memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses. Applicants respectfully submit that the generation of different address spaces allocated for different types of addressing usage, as taught by Campbell, neither teaches nor suggests the mapping of virtual addresses to physical addresses for access to main memory where the physical addresses have a greater number of bits than the virtual addresses as recited by amended Claim 30.

Applicants respectfully submit that the features of amended Claim 30 are neither taught, disclosed or suggested by the combination of Jeddeloh in view of Campbell, as required to establish *prima facie* obviousness. Id. Therefore, Applicants respectfully submit that Claim 30, as amended, is patentable over the combination of Jeddeloh in view of Campbell. Consequently, Applicants respectfully request the Examiner reconsider and withdraw the rejection of Claim 30.

Regarding Claims 31 and 32, Claims 31 and 32, based on their dependency from Claim 30 are also patentable over the combination of Jeddeloh in view of Campbell.

The Examiner has rejected Claims 15, 17 and 19-21 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Campbell and further in view of U.S. Patent No. 5,060,137 issued to Bryg et al. ("Bryg"). Applicants respectfully traverse this rejection.

Regarding Claims 15 and 19, Claims 15 and 19 recite the following analogous claim feature ,which is neither taught nor suggested by the combination of Jeddeloh in view of Campbell and further in view of Bryg:

> control logic coupled to the translation lookaside buffer, the input register and the output register, the control logic to populate entries within the translation lookaside buffer to map virtual addresses of a memory range allocated to the graphic controller to physical addresses within main memory where the physical addresses have a greater number of bits than the virtual addresses. (Emphasis added.)

For at least the reasons previously indicated above with regard to the rejection of Claims 8 and 30, the combination of Jeddeloh in view of Campbell fails to teach or suggest the expansion of a physical address range for axis to main memory by providing a mapping of

virtual addresses to physical addresses where the physical addresses have a greater number of bits than the virtual addresses, as recited by Claims 15 and 19, as amended.

Regarding the Examiner's citing of Bryg, Applicants respectfully submit that the Examiner's citing of Bryg fails to rectify the deficiencies of the combination of Jeddeloh in view of Campbell to teach the control logic coupled to the translation lookaside buffer to populate entries within the translation lookaside buffer to map the virtual addresses of a virtual memory range allocated to the graphics controller to physical addresses within the main memory where the physical addresses have a greater number of bits than the virtual addresses, as recited by Claims 15 and 19, as amended.

Applicants respectfully submit that the references of record are not directed to overcoming the, for example, 4 Gb limit imposed by conventional 32-bit registers and busses. Although Campbell discloses the use of different address spaces for allocation of different types of addressing usage by providing additional bits as part of a physical address, such physical address enables access to the respective device and does not provide access to main memory. As taught by Campbell, a DMA engine allows DMA operations to be performed with respect to the memory device without the need for intervention by CPU 203.

Applicants respectfully submit that the absence within Campbell of any disclosure, teaching or suggestion regarding the DMA engine's use of TLB 204 to expand a received virtual address to a physical address for access to main memory, where the physical address has a greater number of bits than the virtual address, as recited by Claims 15 and 19, prevents the Examiner from establishing a *prima facie* case of obviousness of amended Claims 15 and 19. In re Royka, supra.

Consequently, Applicants respectfully submit that Claims 15 and 19, as amended, are patentable over the combination of Jeddeloh in view of Campbell and further in view of Bryg. Id. Therefore, Applicants respectfully request the Examiner reconsider and withdraw the §103 rejection of Claims 15 and 19.

Regarding Claims 17, 20 and 21, Claims 17, 20 and 21, based on their dependency from Claims 15 and 19, respectively, are also patentable over the combination of Jeddeloh in view of Campbell and further in view of Bryg. Therefore, Applicants respectfully request the Examiner reconsider and withdraw the § 103 rejection of Claims 17, 20 and 21.

CONCLUSION

In view of the foregoing, it is submitted that Claims 8, 9, 12-15, 17, 19-21 and 30-32 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 10, 2006

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
Telephone (310) 207-3800
Facsimile (310) 820-5988/(310) 820-5270

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below

Marilyn Bass 07-13-06
Marilyn Bass DATE